

Guaranteeing Reliability with Thermal Cycling

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Has been involved in the packaging and reliability of electronic equipment for more than ten years. His specialties include best practices in design for reliability, robustness of Pb-free, failure analysis, accelerated test plan development, finite element analysis, solder joint reliability, fracture, and fatigue mechanics of materials.



Thermal Fatigue

- The majority of electronic failures are thermomechanically related*
 - By thermally induced stresses and strains
 - Root caused to excessive differences in coefficient of thermal expansion

*Wunderle, B. and B. Michel, "Progress in Reliability Research in Micro and Nano Region", Microelectronics and Reliability, V46, Issue 9-11, 2006.



A. MacDiarmid, "Thermal Cycling Failures", RIAC Journal, Jan., 2011.



Designing in Reliability, Earlier is Cheaper



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The Typical Weak Links

- Plated Through Holes
 - Usually high aspect ratio plated though holes
 - Rarely microvias unless a manufacturing defect it present
- Solder Joints
 - 2nd Level interconnects, joints used to connect the component to the circuit board
 - 1st Level interconnects, joints used to connect the die to the package







Thermo-Mechanical Fatigue of Solder Joints

• Know your thermal environment

- What are the reliability requirements
- Is the assembly going to be subjected to numerous large temperature variations
 - Kind of subjective "large" actually depends on the component type
 - Really anything that is being used in aerospace or an uncontrolled environment
- Does the assembly feature components with known thermal cycling robustness issues
 - LCCC (leadless ceramic chip carriers)
 - TSOP (thin small outline package) with Alloy 42 lead frames
 - CBGA (ceramic ball grid array)
 - Etc..

• Factors

- Coefficient of thermal expansions
 - Component
 - Printed circuit board

• Stiffness

- Component
- Printed circuit board
- Solder
 - Alloy
 - Joint dimensions

Examples: Desired Lifetime

- Low-End Consumer Products (Toys, etc.)
 - Do they ever work?
- Cell Phones: 18 to 36 months
- Laptop Computers: 24 to 36 months
- Desktop Computers: 24 to 60 months
- Medical (External): 5 to 10 years
- Medical (Internal): 7 years
- High-End Servers: 7 to 10 years
- Industrial Controls: 7 to 15 years
- Appliances: 7 to 15 years
- Automotive:
- Avionics (Civil): 10 to 20 years
- Avionics (Military): 10 to 30 years
- Telecommunications: 10 to 30 years

10 to 15 years (warranty)

Identify Field Environment

- Approach 1: Use of industry/military specifications
 - MIL-STD-810,
 - MIL-HDBK-310,
 - SAE J1211,
 - IPC-SM-785,
 - Telcordia GR3108,
 - IEC 60721-3, etc.
- Advantages
 - No additional cost!
 - Sometimes very comprehensive
 - Agreement throughout the industry
 - Missing information? Consider standards from other industries
- Disadvantages
 - Most more than 20 years old
 - Always less or greater than actual (by how much, unknown)



	W	ORST-CAS	E USE EN	VIRONME	NT			AC	CELERAT	ED TESTI	NG
	Tmin °C	Tmax °C	ΔT ⁽¹⁾ °C	t _D hrs	Cycles/ year	Typical Years of Service	Approx. Accept. Failure Risk %	Tmin °C	Tmax °C	ΔT ⁽²⁾ °C	t _o min
1) CONSUMER	0	+60	35	12	365	1-3	1	+25	+100	75	15
2) COMPUTERS	+15	+60	20	2	1460	5	0.1	+25	+100	75	15
3) TELECOM	- 40	+85	35	12	365	7-20	0.01	0	+100	100	15
4) COMMERCIAL AIRCRAFT	-55	+95	20	12	365	20	0.001	0	+100	100	15
5) INDUSTRIAL & AUTOMOTIVE PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0.1	0	+100	100	15
6) MILITARY GROUND & SHIP	-55	+95	40 &60	12 12	100 265	10	0.1	0	+100	100 & COLD ⁽³⁾	15
7) SPACE leo geo	-55	+95	3 to 100	1 12	8760 365	5-30	0.001	0	+100	100 & COLD ⁽³⁾	15
8) MILITARY AVIONICS a b c	-55	+95	40 60 80 &20	2 2 1	365 365 365 365	10	0.01	0	+100	100 & COLD ⁽³⁾	15
9) AUTOMOTIVE UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	5	0.1	0	+100	100	15
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Industry Testing of Solder Joint Fatigue

- JEDEC
 - Specification body for component manufacturers
- JEDEC JESD47
 - Guidelines for new component qualification
 - Requires <u>2300</u> cycles of 0 to 100C
 - Testing is often done on <u>thin</u> boards
- IPC
 - Specification body for electronic OEMs
- IPC 9701
 - Recommends <u>6000</u> cycles of 0 to 100C
 - Test boards should be <u>similar thickness</u> as actual design





Solder Joint Fatigue

- Elimination of leaded devices
 - Provides lower RC and higher package densities
 - Reduces compliance



Coefficient of Thermal Expansion

- It is unlikely that the designer or end user will be able to influence the component properties
 - Component packaging is typically driven by the die and assembly
 - Passing of JEDEC level package tests
 - May be able to pick parts with different lead frame materials
- Printed wiring board properties
 - Designer can influence printed wiring board properties

- Glass style
- Laminate type
- Copper
- Thickness

Influence of Board Properties

- In the past most electronic packages had CTE values closer to that of copper, 17.6 ppm/°C
- Larger die and smaller packages have driven a reduction in the component CTE, examples:
 - Leadless ceramic chip resistors 5.6 ppm/°C
 - \circ QFN (quad flat no-leads) 8 to 12 ppm/°C
- The CTE of the laminates has decreased over the years
 - The PCB laminate manufactures do not make it easy to determine the CTE of their laminate

Effect of Glass Style

- Realistic target for board CTE is between 15 and 17 ppm/°C
- Most laminate suppliers provide CTExy values

		370HR
	Property	
		Typical Value
Glass Transition Temperatu	ire (Tg) by DSC, spec minimum	180
Decomposition Temperatur	e (Td) @ 5% wt loss	340
T260 Deg C (TMA)		60
T288 Deg C (TMA)		30
CTE Z avia	A. Pre-Tg	45
CTE, Z-axis	B. Post-Tg	230
CTE, X-, Y-axes	A. Pre-Tg	13/14
,,	B. Post-Tg	14/17

• Key concern, these values are typically for a low resin content laminate (46%-50% resin content by weight, 7628 glass style)

- However the most popular laminates have much higher resin contents
 - Higher resin content = higher CTE
 - Lower modulus

Calculations, Example Modulus

Back calculate what the resin only modulus is and compute modulus accounting for glass content Since Fr-4 board has Fibers oriented in both X and Y direction therefore in order to calculate E_x or E_y , we need to combine equation 1 &2.



$$E_{m} = \frac{-\left(V_{f}^{2}E_{f} + 4V_{m}^{2}E_{f} + 4E_{f} - 2V_{f}E_{x,y}\right) \pm \sqrt{\left(V_{f}^{2}E_{f} + 4V_{m}^{2}E_{f} + 4E_{f} - 2V_{f}E_{x,y}\right)^{2} - 4(2V_{m}V_{f})(2V_{m}V_{f}E_{f}^{2} - 4V_{m}E_{f}E_{x,y})}{2(2V_{m}V_{f})}$$
Consider Positive value of \mathbf{E}_{m} as solution.

Effect of Glass Style

- Modulus decreases as resin content increases
- CTE increases as resin content increases
- Copper content plays a significant role
- These values can be now used to predict solder joint fatigue

Glass Styles	Resin Content (Weight %)	Resin Content (Vol %)	
1027	75%	86%]
1037	75%	86%	1
106	72%	84%	
1067	71%	84%	
1035	70%	83%	Pa)
1078	68%	82%	S
1080	64%	79%	Exy
1086	63%	78%	sity
2313	57%	74%	astic
2113	55%	72%	f El
2116	54%	71%	IS 0
3313	54%	71%	dult
3070	50%	68%	Mo
1647	48%	66%	
1651	48%	66%	
2165	48%	66%	
2157	48%	66%	
7628	46%	64%	



Solder Fatigue Model (Modified Engelmaier)

- Modified Engelmaier
 - Semi-empirical analytical approach
 - Energy based fatigue
- Determine the strain range ($\Delta\gamma$)

$$\Delta \gamma = C \frac{L_D}{h_s} \Delta \alpha \Delta T$$

- C is a correction factor, L_D is diagonal distance, α is CTE, Δ T is temperature cycle, h is solder joint height
 - C, function of activation energy, temperature and dwell time

- \circ L_D is on next page
- $\circ \quad \Delta \alpha \text{ is } \alpha_2 \alpha_1$
- $\circ \Delta T$
- h_s defaults to 0.1016 mm (5 mils)

Solder Model (cont.)

• Determine the shear force applied to the solder joint

$$\left(\alpha_2 - \alpha_1\right) \cdot \Delta T \cdot L_D = F \cdot \left(\frac{L_D}{E_1 A_1} + \frac{L_D}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2 - \nu}{9 \cdot G_b a}\right)\right)$$

- F is shear force, L_D is length, E is elastic modulus, A is the area, h is thickness, G is shear modulus, and a is edge length of bond pad
- Subscripts: 1 is component, 2 is board, s is solder joint, c is bond pad, and b is board

- Takes into consideration foundation stiffness and both shear and axial loads
- Leaded models include lead stiffness

Solder Model (cont.)

 Determine the strain energy dissipated by the solder joint

$$\Delta W = 0.5 \cdot \Delta \gamma \cdot \frac{F}{A_s}$$

 Calculate cycles-to-failure (N₅₀), using energy based fatigue models for SAC developed by Syed – Amkor

$$N_f = (0.0019 \cdot \Delta W)^{-1}$$

Energy Based model for SnPb

$$N_f = (0.0006061 \cdot \Delta W)^{-1}$$

Example Fatigue Calculations for a 2512 Resistor

- Low CTE part (Alumina 5.6 ppm/°C)
- Board thickness
 - This highlights wh some component manufactures ma test on thin laminates



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Effect of Lead Material



 Fatigue predictions using Sherlock for TSOP type devices with Copper and Alloy 42 lead frames

Solder Alloy

- Tin Lead solder typically performs better under very high stress thermal cycling conditions
 - Large ceramic devices (stiff parts)
 - Large changes in temperature
- Becoming less of a choice, most high performance parts are pb-free
- SAC alloys tend to do better for moderate thermal cycles

SnPb vs. SAC

- Where does SnPb out perform Pbfree?
- Leadless, ceramic components
 - Leadless ceramic chip carriers (crystals, oscillators, resistor networks, etc.)
 - SMT resistors
 - Ceramic BGAs
- Severe temperature cycles
 - -40 to 125°C
 - -55 to 125°C





SnPb vs. SAC: Resistors



SnPb vs. SAC: TSOP



SnPb vs. SAC: Area Array Devices



Ratio of SAC/SnPb reliability for area array devices as a function of characteristic lifetime of the SAC component

SnPb vs. SAC: Findings

- 2512 Resistors and TSOPs with Alloy42 leadframes have limited lifetimes
 - □ 500 cycles of -40 to 125°C
 - □ 1500 cycles of 0 to 100°C
- Long dwells up to 8 hours would be expected to reduce lifetime between 40 and 60%
- Once long dwell and differences in shape parameters are taken into account, there is likely to be <u>minimal statistical difference between SAC and</u> <u>SnPb in most operating environments</u>

Plated Through Hole Fatigue

When a PCB experiences thermal cycling the expansion/contraction in the zdirection is much higher than that in the x-y plane. The glass fibers constrain the board in the x-y plane but not through the thickness. As a result, a great deal of stress can be built up in the copper via barrels resulting in eventual cracking near the center of the barrel as shown in the cross section photos below.







Plated Through Hole (PTH) Fatigue

- PTH fatigue is the circumferential cracking of the copper plating that forms the PTH wall
- It is driven by differential expansion between the copper plating (~17 ppm) and the out-ofplane CTE of the printed board (~70 ppm)
- Industry-accepted failure model
 - □ IPC-TR-579





IPC TR-579

- Determine stress applied (σ)
 - Assumes perfectly elastic deformation when below yield strength (Sy)
 - Linear stress-strain relationship above Sy

• Determine strain range ($\Delta \epsilon$)

$$\Delta \varepsilon = \frac{\sigma}{E_{Cu}}$$
, for $\sigma < S_y$

$$\Delta \varepsilon = \frac{S_{y}}{E_{Cu}} + \frac{\sigma - S_{y}}{E_{Cu}'}, \text{ for } \sigma > S_{y}$$

IPC-TR-579 (cont.)

- Apply calibration constants
 - $_{\circ}$ Strain distribution factor, K_d(2.5 5.0)
 - 2.5 recommended
 - $_{\circ}$ Quality index, K_Q(0 –10)

$$\Delta \varepsilon_{\rm eff} = \Delta \varepsilon \left(K_{\rm d} \frac{10}{K_{\rm Q}} \right)$$

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Iteratively calculate cycles-to-failure (N_f)

$$N_{f}^{-0.6}D_{f}^{0.75} + 0.9\frac{S_{u}}{E} \left[\frac{\exp(D_{f})}{0.36}\right]^{0.1785\log\frac{10^{5}}{N_{f}}} - \Delta\epsilon = 0$$

Assessment of IPC-TR-579

- Based on round-robin testing of 200,000 PTHs
 - Performed between 1986 to 1988
 - $_{\circ}$ Hole diameters (250 μm to 500 $\mu m)$
 - Board thicknesses (0.75 mm to 2.25 mm)
 - Wall thickness (20 μm and 32 μm)
- Advantages
 - Analytical (calculation straightforward)
 - Validated through testing
- Disadvantages
 - No ownership
 - Validation data is ~18 years old
 - Unable to assess complex geometries (PTH spacing, PTH pads)
 - Complex geometries tend to extend lifetime
 - Difficult to assess effect of multiple temperature cycles
 - Can be performed using Miner's Rule

Factors

• The closer the CTEz value is to copper the better

• Laminate

- Glass style
- Resin

• Tradeoff

- High glass content Harder to drill
- Copper ductility



Exceptions

- The use of underfills, potting compounds and thick conformal coatings can greatly influence the failure behavior under thermal cycling
 - Anytime a material goes through its glass transition temperature problems tend to occur
 - Conformal coating should not bridge between the PCB and the component
 - Underfills designed for enhancing shock robustness do not tend to enhance thermal cycling robustness



Thick Conformal Coating

- Acrylic Conformal Coating
- Verification and determination of mechanical properties
 - Elastic Modulus as a function of temperature
 - Glass Transition
 Temperature
 - Coefficient of Thermal Expansion



Young's Modulus Datasheet 1260 psi (8.7 MPa)

Coefficient of thermal Expansion Datasheet 55 ppm/°C

	Continuous Use Temp. Range °C	- 65 +125
	Thermal Shock Test ⁷	Passes
Ical	Flammability ⁸ (self extinguishing)	Yes
Phys	TCE in/in/°C ⁹	5.5 x 10 ⁻⁵
	Young's Modulus ¹⁰ psi	1260
	Tg ℃ ¹¹	15
	Dielectric Constant ¹²	2.5
_	Dissipation Factor ¹³	.01
ectrica	Dielectric Withstand ¹⁴ (volts)	>1,500
Ē	Insulation Resistance ¹⁵ (teraohms)	800
	Moisture Resistance ¹⁶ (gigaohms)	60



Failure Criteria Definition

The number of cycles to failure is defined to occur at the point when the location of the side of the solder joint is equal to one half the pitch



Reliability

- Underfill is increasingly be considered for PoP and BGAs
 - Improves 2nd level reliability under drop testing
- However, increasing indications that the use of underfill may greatly reduce reliability under temperature cycling
- Example (-40 to 125C)
 - With underfill: 300 cycles
 - Without underfill: >1000 cycles

Reliability: Underfill and Thermal Cycling

Description	Combin	ation A	Combin	ation B
Description	A Bottom A Top		B Bottom	В Тор
No underfill				
Layout 1	4/48	No failure	3/48	4/48
NSMD				
Underfill A				
Layout 1	No failure	No failure	No failure	No failure
NSMD				
Underfill B				
Layout 1	No failure	No failure	No failure	No failure
NSMD				
No underfill				
Layout 3	5/48	No failure	1/48	2/48
SMD				
Underfill B				
Layout 3	No failure	No failure	No failure	No failure
SMD				
Underfill B				
Layout 3	No failure	No failure	No failure	No failure
SMD				

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Table 5. Thermal cycling results after 800 cycles

Decerintion	Combin	nation A	Combin	ation B
Description	A Bottom	А Тор	B Bottom	В Тор
No underfill	No failure	No failure	No failure	No failure
Underfill A	No failure	No failure	2/8	8/8
Underfill B	No failure	No failure	No failure	4/8
Underfill C	No failure	4/8	6/8	7/8



Figure 16. Thermal cycling cracks on top part combination B with underfill C.



Figure 17. Thermal cycling cracks on bottom part combination B with underfill C.

Underfill and Thermal Cycling (cont.)

Underfill name	Dispensing pattern	Filler content (wt%)	Tg by TMA ('C)	CTE, α1 (ppm/'C)	CTE, α2 (ppm/'C)
А	Full	70	113.1	19.9	83
В	Full	0	67.0	61.5	129
С	Corner dot & L	0	123.9	64.7	180
D	Full	0	62.9	69.4	195
E	Full	65	50.3	51.9	181
F	Full	50	60.1	42.8	125
G	Full	0	89.0	58.0	193
Н	Full	0	94.4	59.0	195









Underfill and Temperature Cycling

Underfill name	NBR of failure	1 st failure	MTTF	63.2%, η	Slope, β
No underfill A	8/28 0/30	1968	2727	2858	10.74
В	27/30	555	1334	1481	3.58
C (dot)	20/30	1738	2369	2470	12.22
C (L)	22/30	1832	2470	2348	11.75
D	30/30	202	394	426	5.67
F	30/30	329	512	560	4.75
G	29/30	681	1110	1209	5.02
Н	30/30	270	539	597	3.77

Table 4. Temperature cycling test result summary after 2525 cycles

*data was extrapolated from the test results



 $_{\rm o}$ Rapid time to failure for underfills D / F / G

Best reliability

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• No underfill or underfill with Tg > 110C (A and C) DfR Solutions

Potting

- Materials used for potting
 - Ideally the CTE should be as close to the CCA as possible
 - \circ Usually in the 20 to 30 ppm/°C
 - The larger the CTE the more compliant the potting must be to limit the stresses imparted to the CCA
 - Potting should the generate hydrostatic pressure (equal on all sides) of the circuit card
 - This prevents warping of the CCA as the potting expands
 - Excessive warping will greatly reduce time to failure
 - May cause overstress failures.
 - This may require modification to the housing
 - Housing may need to be relatively stiff to insure this DfR Solutions.

Relating Field to Test

- Back of the envelope technique Norris Landzberg
 - Does not account for part geometries or properties
 - Will give you a general idea of the acceleration factors between the field and test conditions
- More comprehensive
 - Run solder fatigue calculations for the parts
 - Analytical equations
 - Accounts for part and board properties
 - Must be validated against testing
 - Finite Element Analysis

Acceleration Factor Example, JESD47 (Norris Landzberg)

Use Condition	Use Condition Requirement	Equivalent Condition B -55 °C to +125 °C 700 cycles	Equivalent Condition G -40 °C to +125 °C 850 cycles	Equivalent Condition J 0 °C to +100 °C 2300 cycles
Desktop 5 yr Life	ΔT 40 °C 2000 cy	14,175 cy (12,475 cy)* (11,057 cy)**	14,463 cy (12,761 cy)* (11,332 cy)**	14,375 cy (12,675 cy)* (11,250 cy)**
Mobile 4 yr Life	ΔT 15 °C 1500 cy	100,800 cy	102,850 cy	102,221 cy
Server 11 yr Life	ΔT 40 °C 44 cy	14,175 cy	14,463 cy	14,375 cy
Telecom (uncontrolled) / Avionics Controlled 15 yr Life	ΔT 25 °C 5500 cy	36,288 cy	37,026 cy	36,800 cy
Telecom (controlled) 15 yr Life	ΔT 6 °C 5500 cy	630,000 cy	642,812 cy	638,889 cy
Networking 10 year Life	ΔT 30 °C 3000 cy	25,200 cy	25,712 cy	25,557 cy

$$AF = \left[\frac{\Delta T}{\Delta T}\right]^{1.9} \left(\frac{f}{f}\right)^{1/3} \exp\left(1414 \left\{\frac{1}{T_{max}}, \frac{1}{T_{max}}\right\}\right) DfR$$

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Sherlock - Thermal Cycling Fatigue



Cumulative Damage Index (CDI)

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- Time to failure
- Thermal profile

	RefDes	Package	Part Type	Model	Side	Solder	Max dT (C)	Max TSF	Damage 🔹	TTF (yrs)	Score
	U18	TSOP-32 (IC	Leaded	TOP	SAC305	48.3	1.00	2.8E-1	17.68	9.7
1	U14	TSOP-32 (IC	Leaded	TOP	SAC305	47.2	1.00	2.6E-1	18.88	10.0
	U28	TSOP-32 (IC	Leaded	TOP	SAC305	46.3	1.00	2.5E-1	19.88	10.0
	U10	TSOP-32 (IC	Leaded	TOP	SAC305	43.6	1.00	2.1E-1	23.63	10.0
	Х3	SOIC-36 (TRANSDU	Leaded	BOT	SAC305	49.0	1.00	2.1E-1	23.90	10.0
_	U13	TSOP-48 (IC	Leaded	TOP	SAC305	49.5	1.00	1.5E-1	33.57	10.0
	U11	BGA-264	IC	BGA	TOP	SAC305	50.5	1.00	1.3E-1	37.39	10.0
1	U12	BGA-1152	IC	BGA	TOP	SAC305	41.9	1.00	1.3E-1	38.19	10.0
	U7	TSOP-48 (IC	Leaded	TOP	SAC305	45.8	1.00	1.2E-1	41.99	10.0
в	U1	TSOP-48 (IC	Leaded	TOP	SAC305	39.5	1.00	7.9E-2	>50	10.0
na	U29	CFP SOIC	IC	Leaded	BOT	SAC305	36.5	1.00	3.9E-2	>50	10.0
	C33	1206	CAPACITOR	CC	BOT	SAC305	59.8	1.00	1.5E-2	>50	10.0
	U16	PDIP-14 (IC	ThruHole	TOP	SAC305	55.8	1.00	1.3E-2	>50	10.0
	C32	1206	CAPACITOR	CC	BOT	SAC305	57.8	1.00	1.3E-2	>50	10.0
	U15	PDIP-16 (IC	ThruHole	TOP	SAC305	53.5	1.00	1.2E-2	>50	10.0
	C23	1206	CAPACITOR	CC	BOT	SAC305	53.6	1.00	9.6E-3	>50	10.0
	C22	1206	CAPACITOR	CC	BOT	SAC305	53.5	1.00	9.6E-3	>50	10.0
	C21	1206	CAPACITOR	CC	BOT	SAC305	53.3	1.00	9.4E-3	>50	10.0

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Any Questions

